REMARKS

Claim rejections under 35 USC 102

Claims 1-15 have been rejected under 35 USC 102(b) as being anticipated by Coon (6,356,615). Claims 1 and 13 are independent claims, from which the remaining claims rejected on this basis ultimately depend. Applicant submits that claims 1 and 13 are patentable, such that all the claims rejected on this basis are patentable at least because they depend from patentable base independent claims.

Insofar as the rejection over Coon is concerned, Applicant discusses claim 1 as representative of both independent claims 1 and 13. Claim 1 is limited to two elements: a memory array that stores counter values, and a hardware incrementer to read the counter values from the memory array, increment them, and write the counter values as incremented back to the memory array. The memory array is indexable by an index. The hardware incrementer reads the counter values from the memory array by values of this index.

Applicant respectfully submits that the Examiner has not provided a *prima facie* case of anticipation of Coon as to the claimed invention, insofar as he has not indicated which element of Coon corresponds to the memory array of the claimed invention, and which element corresponds to the hardware incrementer of the claimed invention. The Examiner has relied upon column 5, line 65, through column 6, line 5 of Coon as disclosing both the memory array and the hardware incrementer of the claimed invention. This excerpt of Coon just discloses counters 3, 5, 7, and 9, which increment and store counter values.

Applicant submits that the counters of Coon do not correspond to either the memory array of the claimed invention, or the hardware incrementer of the claimed invention, as is discussed in more detail later in this office action response. However, for sake of argument, even if at best the counters of Coon could somehow correspond to the memory array of the claimed invention, then in this case there is no separate element of Coon that corresponds to the hardware incrementer of

the claimed invention, such that Coon still does not anticipate the claimed invention. Likewise, for sake of argument, even if at best the counters of Coon could somehow correspond to the hardware incrementer of the claimed invention, then in this case there is no separate element of Coon that corresponds to the memory array of the claimed invention, such that Coon still does not anticipate the claimed invention.

That is, the Examiner has referenced a single element of Coon – its counters – in the office action, but the claimed invention is limited to two elements: a memory array and a hardware incrementer. Applicant respectfully requests that the Examiner indicate which element of Coon corresponds to the memory array of the claimed invention, and which element corresponds to the hardware incrementer of the claimed invention, with the understanding that these have to be two separate elements in Coon, insofar as the claimed invention is limited to two such separate elements. Otherwise, there is no *prima facie* anticipation of the claimed invention by Coon.

That is, a single element of the prior art cannot be considered as *both* elements of the claimed invention, where the claimed invention is explicitly limited to two different elements. Anticipation requires that a prior art reference disclose each element of the claimed invention "arranged as in the claimed." (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)) A prior art reference teaching a single element cannot be said to anticipate a claim where the claimed invention is limited to two elements, since such a prior art reference does not "arrange" its elements as in the claimed invention. In other words, the "arrangement" of the claimed invention is that there are two elements, whereas the prior art teaches just one element, such that the prior art does not anticipate the claimed invention. "[A]bsence from the reference of any claimed element negates anticipation." (Rowe v. Dror, 112 F.3d 473, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997)

For example, consider the Federal Circuit decision, In re Robertson, 169 F.3d 743, 49 USPQ2d 1949 (Fed. Cir. 1991). In Robertson, the claim at issue was directed to a diaper that included three fastening means. However, the prior art reference in question disclosed a diaper

that only had two fastening means. The Federal Circuit held in Robertson that the Board erred in concluding that the prior art reference anticipated the claimed invention. "[T]he Board failed to recognize that the third mechanical fastening means in claim 76 . . . was separate from and independent of the two other mechanical means used to attach the diaper to the person." (Id. at 1951) "The Board's theory that these two fastening devices in [the prior art reference] were capable of being intermingled to perform the same function as the third and first fastening elements in claim 76 is insufficient." (Id.)

Applicant further submits, however, that the counters of Coon do not correspond to the memory array of the claimed invention, or the hardware incrementer of the claimed invention. With respect to the memory array, the claimed invention is limited to such a memory array storing counter values that are indexable by an index. The counters of Coon are selectable by multiplexers (MUX's) 27, 29, 31, and 33. (Col. 3, ll. 56-65) However, the counters are not a "memory array," as this term can most broadly be construed by those of ordinary skill within the art. Rather, the counters of Coon are simply that – counters – and not an array of memory, to which the claimed invention is limited. For this reason as well, Coon does not anticipate the claimed invention.

With respect to the hardware incrementer, the claimed invention is limited to such a hardware incrementer that reads counter values from a separate element – the memory array – increments the counter values, and writes them back into the memory array. The counters of Coon are in the first instance not hardware incrementers, but hardware *decrementers*, in that they "are configured to decrement from a set number." (Col. 5, ll. 65-66) Furthermore, the counters of Coon are not described as reading their values from a separate element, a memory array, nor writing these values back to the separate element after incrementation. Rather, it appears that the counters decrement their counter values as stored within the counters themselves (see, e.g., col. 5, l. 65, through col. 6, l. 5), as opposed to having to read the values from a separate element, a

memory array, performing decrementation, and writing the values back to this separate element. Therefore, Coon does not anticipate the claimed invention for this reason, too.

Claim rejections under 35 USC 103

Claims 16-17 and 19-20 have been rejected under 35 USC 103(a) as being unpatentable over Coon in view of Intel News Release ("Intel"). Claim 16 is an independent claim, from which claims 17 and 19-20 ultimately depend. Applicant submits that claim 16 is patentable over Coon in view of Intel, such that all the claims 16-17 and 19-20 are patentable over Coon in view of Intel.

Claim 16 is limited to a system in which a performance counter has "a lesser number of hardware incrementers than a number of . . . events of which the performance counter counts . . . occurrences." The Examiner has stated that Coon discloses this limitation of claim 16, such that Coon in view of Intel renders the invention of claim 16 obvious and unpatentable. Applicant respectfully disagrees. In explaining why, Applicant concentrates on Coon not disclosing this limitation in arguing that Coon in view of Intel does not teach all the limitations of the claimed invention, insofar as the Examiner has concentrated on Coon as disclosing this limitation in arguing that Coon in view of Intel does teach all the limitations of the claimed invention.

The limitations of claim 16 specify that the number of hardware incrementers is less than the number of events that the performance counter counts occurrences of. For example, there may be one hardware incrementer, but two events. The performance counter of which the hardware incrementer is a part thus is able to count the occurrence of each of these events. The first event may occur three times, such that the performance counter counts that the first event has occurred three times. The second event may occur nine times, such that the performance counter counts that the second event has occurred nine times. That is, the performance counter maintains two counter values in this example, one for each of the two different events, even though the performance counter has just one hardware incrementer in this example to actually increment the

counter values. The two counter values (as may be stored in a memory array, for instance) can be accessed separately/independently.

By comparison, in Coon each hardware incrementer corresponds to one counter value. For instance, each of the counters is input with a desired number, and each time an input is received, the corresponding number decreases. (Col. 5, l. 65, through col. 6, l. 6) Now, what Coon does disclose is that each hardware incrementer can count occurrences of *combinations of events*. For instance, in column 5, lines 29-30 and 54-67, Coon discloses that signal combiners combine "events from two of the individual functional units," such that these events "may be combined." Column 7, lines 46-53 of Coon provides an example in which events X and Y are combined, such that when both are true, a count is made. However, even though there are two events, there is just a single count value – the hardware incrementer in Coon counting in this example occurrences of both the events X and Y occurring. That is, Coon does not count occurrences of the event X as well as occurrences of the event Y (as two separate count values), but rather counts occurrences of the combination of the events X and Y (as a single count value).

Consider also the example discussed above, but in relation to Coon, where there is one hardware incrementer and two events. Such a hardware incrementer of Coon can count the occurrences of the first event, *OR* the occurrences of the second event, *OR* the occurrences of both the first and the second events at the same time (or any other Boolean combination of the first event and the second event). That is, Coon has just one counter value in this example, since it has just one hardware incrementer. By comparison, the claimed invention in this example allows a *single* hardware incrementer to count occurrences of the first event, *AND* occurrences of the second event. Even though the claimed invention has just one hardware incrementer in this example, it can maintain *two* counter values, one corresponding to occurrences of each event. Coon cannot do this. Rather, Coon can maintain a single counter value, corresponding to occurrences of the first event, *OR* occurrences of the second event, *OR* occurrences of any combination of the first and the second events.

In this respect, Coon does not have "a lesser number of hardware incrementers than a number of . . . events of which the performance counter counts . . . occurrences," as to which the claimed invention is limited. Therefore, Coon in view of Intel does not render the claimed invention obvious and unpatentable.

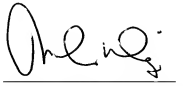
Allowed claims

Claim 18 has been indicated as containing allowable subject matter, and which would be allowed if rewritten in independent form, including the limitations of its base claim and any intervening claims.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mike Dryja, Applicants' Attorney, at 425-427-5094, so that such issues may be resolved as expeditiously as possible. For these reasons, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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